In the Claims:

Please amend claims 1, 7 and 12 as follows:

Sub C1

1. (Amended) A semiconductor memory device, comprising:

a semiconductor substrate, a gate electrode formed on the semiconductor substrate, and a plurality of source/drain junctions formed in the semiconductor substrate;

A1

an interlayer insulating layer formed over the semiconductor substrate;

a plug formed in the interlayer insulating layer, the plug includes a diffusion barrier layer and a seed layer for electro plating;

a lower electrode of a capacitor contacted to the seed layer;

a dielectric layer formed on the lower electrode; and

an upper electrode formed on the dielectric layer.

Sub C2

7. (Amended) A method for fabricating semiconductor memory device, comprising the steps of:

A2

providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the

semiconductor substrate;

etching the interlayer insulating layer and forming a contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a lower electrode of a capacitor contacted to the seed layer by using an electro plating technique;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.

12. (Amended) A method for fabricating semiconductor memory device, comprising the steps of:

providing a semiconductor substrate, forming a gate electrode on the semiconductor substrate, and forming a plurality of source/drain junctions in the semiconductor substrate;

forming an interlayer insulating layer over the semiconductor substrate;

etching the interlayer insulating layer and forming a contact hole;

forming a plug in the contact hole, wherein the plug includes a diffusion barrier layer and a seed layer for electro plating;

forming a glue layer on the seed layer and the interlayer insulating layer;

forming a sacrificial layer on glue layer;

etching the sacrificial layer and the glue layer and forming an opening defining a region of a lower electrode of a capacitor;

forming the lower electrode on the seed layer in the opening, by using an electro plating technique;

removing the sacrificial layer and the glue layer;

forming a dielectric layer of the capacitor on the lower electrode; and

forming an upper electrode of the capacitor on the dielectric layer.